WHAT IS CLAIMED IS:

1. A method comprising:

placing underfill material on a first side of a first integrated circuit die, the first side of the first integrated circuit die comprising a first plurality of electrical contacts; and

placing a first side of a second integrated circuit die on the underfill material, the first side of the second integrated circuit die comprising a second plurality of electrical contacts.

2. A method according to Claim 1, further comprising:

applying energy to the underfill material and to the first and second plurality of electrical contacts to electrically couple ones of the first plurality of electrical contacts and respective ones of the second plurality of electrical contacts, and to cure the underfill material.

3. A method according to Claim 2, wherein applying the energy comprises:

applying energy to first electrically couple ones of the first plurality of electrical contacts and respective ones of the second plurality of electrical contacts, and to then cure the underfill material.

4. A method according to Claim 2, wherein applying the energy comprises:

applying energy to the underfill material to perform fluxing on one or more of the first plurality of electrical contacts and on one or more of the second plurality of electrical contacts.

5. A method according to Claim 1, further comprising:

bonding a second side of the first integrated circuit die to a substrate.

6. A method according to Claim 5, wherein the second side of the first integrated circuit die comprises a third plurality of electrical contacts, wherein the substrate comprises a fourth plurality of electrical contacts, and wherein bonding the second side of the first integrated circuit die to the substrate comprises:

placing second underfill material on the substrate;

placing the second side of the first integrated circuit die on the second underfill material; and

applying second energy to the second underfill material and to the third and fourth plurality of electrical contacts to electrically couple ones of the third plurality of electrical contacts and respective ones of the fourth plurality of electrical contacts, and to cure the second underfill material.

7. A method according to Claim 5, wherein the second side of the first integrated circuit die comprises a third plurality of electrical contacts, wherein the substrate comprises a fourth plurality of electrical contacts, and wherein bonding the second side of the first integrated circuit die to the substrate comprises:

applying flux to the fourth plurality of electrical contacts;

placing the second side of the first integrated circuit die on the substrate;

applying second energy to the third and fourth plurality of electrical contacts to electrically couple ones of the third plurality of electrical contacts and respective ones of the fourth plurality of electrical contacts;

placing second underfill material on the substrate; and

applying third energy to the second underfill material to promote capillary flow of the second underfill material between the first integrated circuit die and the substrate, and to cure the flowed second underfill material.

8. A method according to Claim 1, wherein the first side of the second integrated circuit die comprises first integrated devices.

9. A method according to Claim 8, wherein a second side of the first integrated circuit die comprises second integrated devices.

10. A method according to Claim 1, wherein the underfill material is no-flow underfill material.

11. A method according to Claim 1, wherein a length and a width of the second integrated circuit die are substantially equal to a length and a width of the first integrated circuit die.

12. A method according to Claim 1, wherein a length of the second integrated circuit die is greater than a length of the first integrated circuit die, and wherein a width of the second integrated circuit die is greater than a width of the first integrated circuit die.

13. A device comprising:

a first integrated circuit die, a first side of the first integrated circuit die comprising a first plurality of electrical contacts;

no-flow underfill material in contact with the first side of the first integrated circuit die; and

a second integrated circuit die, a first side of the second integrated circuit die comprising a second plurality of electrical contacts, and the first side of the second integrated circuit die in contact with the no-flow underfill material.

14. A device according to Claim 13, the first integrated circuit die comprising a second side, the device further comprising:

second underfill material in contact with the second side of the first integrated circuit die; and

a substrate in contact with the second underfill material.

15. A device according to Claim 14,

wherein the second side of the first integrated circuit die comprises a third plurality of electrical contacts,

wherein the substrate comprises a fourth plurality of electrical contacts, and

wherein ones of the fourth plurality of electrical contacts are electrically coupled to respective ones of the third plurality of electrical contacts.

16. A device according to Claim 14, wherein the second underfill material comprises no-flow underfill material.

17. A device according to Claim 14, wherein the second underfill material comprises capillary flow underfill material.

18. A device according to Claim 13, wherein the no-flow underfill material comprises fluxing functional groups.

19. A device according to Claim 13, wherein the first side of the second integrated circuit die comprises first integrated devices.

20. A device according to Claim 19, wherein a second side of the first integrated circuit die comprises second integrated devices.

21. A device according to Claim 13, wherein a length and a width of the second integrated circuit die are substantially equal to a length and a width of the first integrated circuit die.

22. A device according to Claim 13, wherein a length of the second integrated circuit die is greater than a length of the first integrated circuit die, and wherein a width of the second integrated circuit die is greater than a width of the first integrated circuit die.

23. A device according to Claim 13, wherein the second integrated circuit die comprises a memory cache.

24. A system comprising:

a microprocessor comprising:

a first integrated circuit die, a first side of the first integrated circuit die comprising a first plurality of electrical contacts;

no-flow underfill material in contact with the first side of the first integrated circuit die; and

a second integrated circuit die, a first side of the second integrated circuit die comprising a second plurality of electrical contacts, and the first side of the second integrated circuit die in contact with the no-flow underfill material; and

a double data rate memory electrically coupled to the microprocessor.

25. A system according to Claim 24, the first integrated circuit die comprising a second side, the system further comprising:

second underfill material in contact with the second side of the first integrated circuit die; and

a substrate in contact with the second underfill material.

26. A system according to Claim 25,

wherein the second side of the first integrated circuit die comprises a third plurality of electrical contacts,

wherein the substrate comprises a fourth plurality of electrical contacts,

wherein ones of the fourth plurality of electrical contacts are electrically coupled to respective ones of the third plurality of electrical contacts, and

wherein ones of the fourth plurality of electrical contacts are electrically coupled to the memory.

27. A system according to Claim 24, wherein the second integrated circuit die comprises a memory cache.

28. A system according to Claim 24, wherein a length and a width of the second integrated circuit die are substantially equal to a length and a width of the first integrated circuit die.

29. A system according to Claim 24, wherein a length of the second integrated circuit die is greater than a length of the first integrated circuit die, and wherein a width of the second integrated circuit die is greater than a width of the first integrated circuit die.